



Malla Reddy Engineering College

(AUTONOMOUS)

(An UGC Autonomous Institution approved by AICTE and affiliated to JNTU Hyderabad, Accredited by NAAC with 'A' Grade (II - cycle)
NBA Accredited Programmes - UG (CE, EEE, ME, ECE & CSE) PG (CE - Structural Engg., EEE-Electrical Power Systems, ME - Thermal Engg.).

ORDER

Date: 31.03.2015

The ECE UG-Board of Studies for the Academic year 2015-16 have been reconstituted as per the UGC guidelines.

S. No.	Name of the Member	Designation & Official Address	Subject Specialization	Contact No.	Status
1	Dr. S. Sudhakara Reddy	Principal & Constituted BoS	Mechanical Engineering	9348161125	Special Invitee
2	Dr. M.J.C.Prasad	Chairman- BoS Professor & HOD-ECE	Digital Signal Processing	8019914846	Existing Member
3	Dr. B.N.Bandari	Professor ,ECE Department JNTUHCEH	Communication Engineering	9441189228	Nominee of JNTUHCEH
4	Dr. N. S. Murthy	Rtd.Professor,ECE Dept. NIT Warangal	VLSI & Signal Processing	08702459234	Existing Member
5	Dr. K. Jaya Sankar	Professor & HOD, Dept. of ECE, Vasavi Engineering College,Hyderabad	Communication Engineering	9440162196	New Member
6	D.Srikanth,	Manager(Technical), Advanced Micro Devices(AMD) Ltd, Hyderabad & Industry Expert	VLSI	9912333452	New Member
7	Dr.Kesavan Gopal	Professor, ECE Department, MREC	VLSI	9000368726	New Member
8	Prof.Jakeer Hussain	Assoc. Professor, ECE Department, MREC	Digital Systems	9866875459	New Member
9	Mr. P.Ashok Babu	Assoc. Professor, ECE Department, MREC	Communications & Image Processing	9848898290	Existing Member
10	Mrs.P.S.Indrani	Assoc. Professor, ECE Department, MREC	DSCE	9490224344	Existing Member
11	Mr.B.Srinivas	Assoc. Professor, ECE Department, MREC	Embedded Sydtms	9966764588	Existing Member
12	Ms.P.Vasanthi	Deputy Engineer, BEL, Bangalore	Microwave & Radar	09740123084	Alumni Member



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Department of Electronics and Communication Engineering

14/04/2015

AGENDA

- 1 Finalization of Schema & Syllabus for B.Tech Course for the Academic Year 2015-16
- 2 Finalization of Schema & Syllabus for M.Tech(DSCE), M.Tech(VLSI System Design) and M.Tech(ES) Courses for the Academic Year 2015-16.
- 3 Identification of Examiners and Valuers list.
- 4 Finalization of one common subject for Non ECE Branch Students as Elective.
- 5 Any other point

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BoS Chairman-ECE

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**MALLA REDDY ENGINEERING COLLEGE
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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

The BOS meeting is held on 14/04/2015 and the following members have attended for finalization of Schema and Syllabus for both B.Tech and M.Tech.

S. No.	Name of the Member	Designation & Official Address	Signature
1	Dr. S. Sudhakara Reddy	Principal & Constituted BoS	
2	Dr. M. Ch. P. Jagdish	Chairman- BoS Professor & HOD-ECE	
3	Dr. D. Srinivasa Rao	Professor & BOS Chairman - ECE- JNTUHCEH	
4	Dr. N. S. Murthy	Dean & Professor of ECE- NIT Warangal	
5	Mr.K.Srinivasa Raju	CEO, Unistring Tech Solutions(pvt) Ltd, Hyderabad & Industry Expert	
6	Dr. K. Jaya Sankar	Profesor & Head, Dept. of ECE, Vasavi Engineering College, Hyderabad	
7	Dr. Kesavan Gopal	Professor, ECE Department, MREC	
8	Mr. P. Ashok Babu	Assoc. Professor, ECE Department, MREC	
9	Mrs. P. S. Indrani	Assoc. Professor, ECE Department, MREC	
10	Mr. B. Srinivas	Assoc. Professor, ECE Department, MREC	
11	Ms. P. Vasanthi	MREC Alumni Presently Deputy Engineer, BEL, Bangalore	



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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MINUTES OF BOS MEETING HELD ON 14TH April 2015 IN ECE DEPARTMENT

1. The Structure and Syllabus for B.Tech MR15 batch have been approved with the following suggestions

Year	Semester	Name of the Subject	Modifications Suggested
II	I	Electronic Circuit Analysis	“Small stage amplifiers” topic is added.
II	I	Signal and Systems	Unit-III and Unit –IV are interchanged and the syllabus of “Fourier series” topic is to be reduced. Introduction to Signal Unit is added
II	I	Probability Theory And Random Processes	New unit introduced: Unit V- Linear System with random Input.
II	I	Basic Simulation lab	Simple circuit simulation experiments using NSPICE are to be introduced.
II	II	Pulse and Digital Circuits	“RTL, DCTL, DTL” topics are to be removed.
II	II	NW & TL	EMTL subject is divided into two separate subjects namely EM Theory and Networks & transmission Lines. Network Topology from EC is to be included as one Unit Network Functions and Filters & Symmetrical Attenuators from PEE are to be included as Two Units. Two Units from EMTL i.e Transmission Lines are to be included as Two Units.
II	II	PDC Lab	New programs are added 1 HDL Code to Realize all the logic gates 2 Design of 2 to 4 Decoder 3 Design of 8 to 1 multiplexer & 1*8 Demultiplexer 4 Design of flip flops: SR,D,JK,T
II	II	EM Theory	Three Units from EMTL are to be arranged as Five Units in EM Theory.
III	I	LICA	LDICA Subject is divided into two separate subjects namely LICA and DICA.
III	I	DICA	The concepts of verilog in DDUV are to be added. Basics of FPGA’s are to be added in DICA.
III	II	Digital Signal Processors	DSP Processor topic is added in V Unit
IV	I	DIP	DIP is to be replaced by Digital Image & Video Processing in Elective-I.

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IV	I	CTT	TVE is to be replaced by CTT in Elective-II.
IV	II	Speech Signal Processing.	ANN subject is to be replaced by Speech Signal Processing in Elective-III
IV	II	Ad-Hoc Wireless Sensor Networks	Instead of Multimedia and Signal Coding subject Ad-Hoc Wireless Sensor Networks is to be added in Elective-I

2. The structure and syllabus for M. Tech DSCE, M.Tech VLSI System Design & M.Tech ES have been approved with few modifications as follows .

The syllabus for M. Tech subject “VLSI Technology and Design” is modified.

3. After formulation of scheme of Instructions, the BOS members reviewed and approved new courses for **B.Tech ECE**

The following subjects are introduced for the academic year 2015-16 (MR15).

Elementary Calculus and Transforms
 Special Functions and Complex Analysis
 Microprocessor and Interfacing
 Technical Communication and Presentation Skills
 Microprocessor and Interfacing Lab
 Technical Communication and Presentation Skills Lab
 Engineering Economics And Accountancy
 Engineering Economics and Accountancy
 Microcontrollers and Embedded Systems
 Microcontrollers Lab
 Soft Skills
 Advanced Microcontrollers
 Hardware Software Co-Design
 Advanced Digital Signal Processing
 Introduction to Nano Science and Nano Technology
 Design For Testability
 Digital Signal Processors and Architectures
 Low Power VLSI Design
 Entrepreneurship Skills
 Foreign Language /Fine Arts

- 4 .Open elective subject “ Principles of Communication Engineering ” is introduced for non ECE branch Students.

- 5 After formulation of scheme of Instructions, the BOS members reviewed and approved new courses for **M.Tech DSCE**

The following subjects are introduced for the academic year 2015-16 (MR15)

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Hardware and Software Co-Design

Design Of Fault Tolerant System

Nano Electronics

Real Time Operating Systems

Device Modeling

Software Define Radio

Ad Hoc Wireless Networks

Scripting Language

6 After formulation of scheme of Instructions, the BOS members reviewed and approved new courses for **M.Tech VLSI System Design**

The following subjects are introduced for the academic year 2015-16 (MR15)

Hardware Description Language

Algorithm for VLSI Design Automation

Embedded system Design

Soft Computing Techniques

Image and Video Processing

Coding Theory and Techniques

VLSI and DSP Architecture

Full Custom IC Design

Software Defined Radio

Ad Hoc Wireless Network


7 After formulation of scheme of Instructions, the BOS members reviewed and approved new courses for **M.Tech ES**

The following subjects are introduced for the academic year 2015-16 (MR15)

ARM Architecture

Digital System Design

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Design for Testability

TCP/IP Networks

Coding Theory and Techniques

CPLD and FPGA Architecture and Applications

Wireless Communication and Networks

Scripting Language

Device Modeling



Chairman-BOS

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